307, and around the annular gate 307 and the annular gate dielectric layer 306; and performing an etch back process to remove the sidewall spacer material layer on the semiconductor substrate 301 and the annular gate 307. Thus, the sidewall spacers 308 on the side surfaces of the annular gate 307 and the annular gate dielectric layer 306 may be formed.

The sidewall spacer material layer may be made of any appropriate material, such as silicon oxide, silicon nitride, or silicon oxynitride, etc. The sidewall spacers 308 may also be stacked layers made of different materials. Various processes may be used to form the sidewall spacer material layer, such as a CVD process, a PVD process, or an ALD process, etc. The etch back process may be a dry etching process, or a wet chemical etching process, etc.

Returning to FIG. 27, after forming the sidewall spacer 308, a source region and a drain region may be formed (S105). FIG. 16 illustrates a corresponding semiconductor structure; and FIG. 17 illustrates a cross-section view of the semiconductor structure illustrated in FIG. 16 along the B-B direction.

As shown in FIG. 16 and FIG. 17, a source region 309 is formed in the lightly doped region 310, and a drain region 305 is formed in the well region 302 at the outer side of the isolation structure 304. Thus, the drain region 305 is an annular shape. Referring to FIG. 17, a depth of the source region 309 may be smaller than a depth of the lightly doped region 310. The source region 309 and the annular drain region 305 may be formed by any appropriate process, such as an ion implantation process, or an embedding method, etc.

The LDMOS transistor may include an annular gate 307, a source region 309 in the lightly doped region 310 at the inner side of the annular gate 307, and an annular drain region 305 in the drifting region 303 at the outer side of an annular isolation structure 304. An annular channel may be formed between the source region 309 and the annular drain region 305. The annular gate 307 may control the annular channel from different directions, thus the LDMOS transistor may have an enhanced channel control ability. Therefore, a short-channel effect may be effectively reduced, and the drive current may be increased. Further, the LDMOS transistor may occupy less area of a chip under a same drive current, thus the production cost may be reduced.

Thus, a LDMOS transistor may be formed by the above disclosed processes and methods, the corresponding LDMOS transistor is illustrated in FIG. 16; and FIG. 17 illustrates a cross-section view of the LDMOS transistor shown in FIG. 16. The LDMOS transistor includes a semiconductor substrate 301 having a well region 302 and an annular drifting region 303 in the well region 302. The LDMOS transistor also includes a source region 309 in a lightly doped drain region 310, and an annular gate dielectric layer 306 and an annular gate 307 surrounding the source region 309. Further, the LDMOS transistor includes an annular isolation structure 304 in the annular drifting region 303 at the outer side of the annular gate dielectric layer 306. Further, the LDMOS transistor also includes sidewall spacers 308 around the annular gate dielectric layer 306 and the annular gate 307, and an annular drain region 305 in the annular drifting region 303 at the outer side of the sidewall spacers 308. The detailed structures and intermediate structures are described above with respect to the fabrication methods.

FIGS. 18, 20, 22 and 24 illustrate semiconductor structures corresponding to certain stages of the exemplary fabrication process of another LDMOS transistor; and FIGS. 19, 21, 23 and 25 illustrate cross-section views of FIGS. 18, 20, 22 and 24 along the C-C direction. For illustrated purposes, the exemplary fabrication process shown in FIG. 27 is still used to make the LDMOS transistor.

As shown in FIG. 27, at the beginning of the fabrication process, a semiconductor substrate with certain structures is provided (S101). FIG. 18 illustrates a corresponding semiconductor structure; and FIG. 19 illustrates a cross-section view of the semiconductor structure shown in FIG. 18 along the C-C direction.

As shown in FIG. 18 and FIG. 19, a semiconductor substrate 401 is provided. The semiconductor substrate 401 may include any appropriate type of semiconductor material, such as single crystal silicon, germanium, poly silicon, amorphous silicon, silicon germanium, carborundum, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, alloy semiconductor, or epitaxially grown materials, etc. The semiconductor substrate 401 may also provide a base for subsequent processes and structures.

After providing the semiconductor substrate 401, a well region 402 may be formed in the semiconductor substrate 401. The well region 402 may be made of any appropriate material, which may be same as the semiconductor substrate 401, or different from the semiconductor substrate 401. If the semiconductor substrate 401 is used to subsequently form N-type LDMOS transistors, the semiconductor substrate 401 may be doped with P-type ions, and the well region 402 may be doped with P-type ions too. If the semiconductor substrate 301 is used to subsequently form P-type LDMOS transistors, the semiconductor substrate 401 may be doped with N-type ions, and the well region 402 may be doped with N-type ions as well. The well region 402 may be formed by any appropriate process, such as an ion implantation process, or an embedding process, etc.

Returning to FIG. 27, after providing the semiconductor substrate 401 with the well region 402, a plurality of annular isolation structures and a plurality of drifting regions may be formed in the well region 402 (S102). FIG. 20 illustrates a corresponding semiconductor structure; and FIG. 21 illustrates a cross-section view of the semiconductor structure shown in FIG. 12 along the C-C direction.

As shown in FIG. 20 and FIG. 21, at least one first annular isolation structure 404' and at least one second annular isolation structure 404 are formed in the well region 402. The second annular isolation structure 404 may surround the first annular isolation structure 404'. Further, a first drifting region 403' and a second drifting region 403 are also formed in the well region 402. The first annular isolation structure 404' may be in the first drifting region 403', and the second annular isolation structure 404 may be in the second drifting region 403. The second drifting region 403 may be an annular drifting region.

In one embodiment, the first drifting region 403' and the second drifting region 403 may be formed in the well region 402 firstly, and then the first annular isolation structure 404' and the second annular isolation structure 404 may be formed in the first drifting region 403' and the second drifting region 403, respectively. In certain other embodiments, the first annular isolation structure 404' and the second annular structure 404 may be formed firstly, and then the first drifting region 403' and the second drifting region 403 may be formed. A doping type of the first drifting region 403' and the second drifting region 403 may be opposite to a doping type of the well region 402. That is, if the well region 402 is N-type doped, the first drifting region 403' and the second drifting region 403 may be doped with P-type